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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Philip L. Hower, et al.	Docket No:	TI-30010
Serial No:	10/036,323	Conf. No:	3224
Examiner:	Thomas L. Dickey	Art Unit:	2826
Filed:	12/31/2001		
For:	N-CHANNEL LDMOS WITH BURIED P-TYPE REGION TO PREVENT PARASITIC BIPOLAR EFFECTS		

APPEAL BRIEF UNDER 37 C.F.R. 1.192

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MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 12-12-03.

Ann Trent
Ann Trent

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed July 30, 2003, and the Advisory Action mailed October 29, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

Claims 1-13, 15, and 19-26 have been canceled. Claims 27-32 have been withdrawn. Claims 14, 16 and 18 are appealed.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

Claim 17 was amended after the final rejection. In an action dated 10/29/2003, the examiner stated that claim 17 as amended would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claims.

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

The instant invention describes a LDMOS transistor with an improved safe operating area. As shown in Figure 1 of the instant disclosure, a p-type buried body is formed beneath the source region 18 and the channel region. The channel region is represented by the region directly beneath the gate from the edge of the n+ source region 18 to the edge of the p body 20 adjacent to the isolation region 28. The n+ drain region 16 is separated from the edge of the channel region by a portion of the n-well 12.

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

1. Was claim 14 properly rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,437,399)?

2. Were claims 16 and 18 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (6,437,399) in view of Mena et al. (4,922,327)?

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

Claims 14, 16, and 18 stand or fall together.

Arguments

1. Was claim 14 properly rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,437,399)?

Appellants contend that claim 14 was not properly rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,437, 399). Claim 14 of the instant invention comprises the limitations of an n-type source diffusion, a p-type surface body diffusion which laterally surrounds at least part of said source diffusion, a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein, and a p-type buried body diffusion which underlies said channel and at least part of said surface body diffusion. In forming the rejection to claim 14, the examiner refers to region 35 as defining a p-type buried body diffusion which underlies a channel. The examiner, in the action dated 10/29/2003, defines the channel in the Huang patent (6,437,399) as being the P-type impurity region 14. This is an overbroad definition of the term "channel region" as used in claim 14 of the instant invention. The "channel region" in claim 14 is formed by, "a conductive gate structure which is capacitively coupled to part of said p–type surface body diffusion to define a channel region therein." The "channel region" of the instant invention is therefore formed when the appropriate voltages are applied to the conductive gate structure and will be confined by the existing electric fields to regions directly beneath the conductive gate structure. This definition of "channel region" coincides with the well established use of the term in semiconductor physics. Appendix I contain the pages from "Physics of Semiconductor Devices" by Sze which provide an explanation of the formation of the "channel region" and its confinement to regions beneath the conductive gate. In particular pages 433 to 445 provide the physics behind the formation of the "channel region" and Fig. 3 and Fig. 6 show the confinement of the "channel region" to the region directly beneath the conductive gate. This is also illustrated in Fig. 19 where the "channel region" is shown for various types of transistors. It should also be noted that claim 14 comprises the limitation of p-type surface body diffusion and a separate "channel region."

In describing the Huang patent, the examiner refers to region 14 in Figure 12 as a p-type surface body diffusion which laterally surrounds at least part of said source diffusion. In the action dated 10/29/2003, the examiner further explains that region 14 (which the examiner had previously equated to the p-type surface body diffusion) is now the channel region. The examiner quotes a section of the Huang patent which states "[t]he region pf P-type impurity 14, generally referred to as the base region, is herein referred to as the channel region because it is the region in which the channel forms during the operation of the device." It is a well established tenet of patent law that a patent can be its own lexicographer. In the above quoted section of the Huang patent, the patent outlines a "new" definition for the term "channel region" that is different from the well established meaning of the term as it is used in claim 14 of the instant invention. With regard to the Huang patent, examination of Figure 12 shows that the actual "channel region" as the term is used in claim 14 (i.e. the region where the channel is formed when the appropriate voltages are applied to the gate 26) extends from the edge of the N+ diffusion region 16 laterally under the gate 26 to the N type drain region. The P+ diffusion region 35 described by the examiner is positioned solely under the N+ source region 16 and does not extend under the "channel region." Therefore the term "channel region" as used in claim 14 is different from the "new" defined meaning of the term as used in the Huang patent. The "new" defined meaning of the term "channel region" applies only to the Huang patent and certainly cannot supercede the well established definition presented in Appendix I and followed in Claim 14. The examiner also refers to claim 10 in the Huang patent where it states "said channel region overlying and boarding a region of high impurity concentration." The term "channel region" in claim 10 of the Huang patent again refers to the "new" definition of the term "channel region" presented in the Huang patent.

All the limitations of claim 14 are not contained in the Huang patent and claim 14 is allowable over the cited art under 35 U.S.C. 102(e).

2. Were claims 16 and 18 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (6,437,399) in view of Mena et al. (4,922,327)?

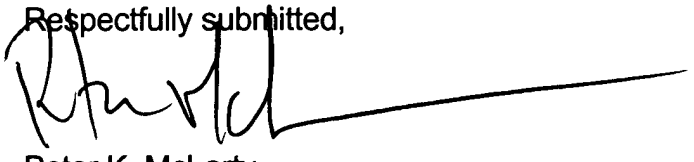
Claims 16 and 18 depend from claim 14 and therefore contain all the limitation of claim 14. The Mena et al. patent does not describe a p-type buried body diffusion which underlies said channel. As described above the Huang patent does not contain this limitation and therefore claims 16 and 18 are allowable over the Huang patent in view of the Mena et al. patent under 35 U.S.C. 103(a).

Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 14, 16, and 18 under 35 U.S.C. § 102 and 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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Attorney for Appellants

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Dallas, Texas 75265
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APPENDIX

Claims on Appeal

Claim 14: An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion, ohmically connected to a source metallization;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein;

a p-type buried body diffusion which underlies said channel and at least part of said surface body diffusion; and

an ohmic connection between said buried body diffusion and said source metallization;

whereby said buried body diffusion diverts hole current to bypass said source diffusion, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device.

Claim 16: The structure of Claim 14, further comprising a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

Claim 18: The structure of Claim 14, further comprising a drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion, and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

APPENDIX I

Physics of Semiconductor Devices

SECOND EDITION

S. M. Sze

Bell Laboratories, Incorporated
Murray Hill, New Jersey

A WILEY-INTERSCIENCE PUBLICATION

JOHN WILEY & SONS

New York • Chichester • Brisbane • Toronto • Singapore

Library of Congress Cataloging in Publication Data:

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"A Wiley-Interscience publication."
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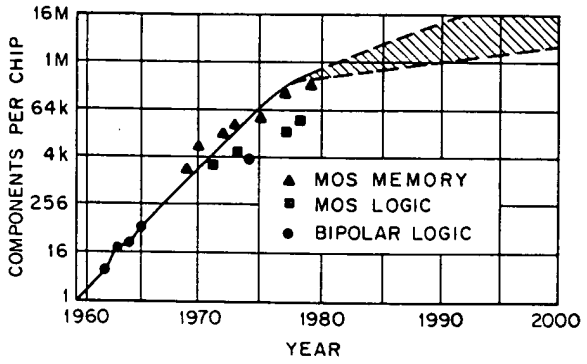

Fig. 2 Complexity of integrated circuits as a function of the year. (After Moore, Ref. 15.)

chip has grown exponentially[15] since 1959 (Fig. 2). The rate of growth is expected to slow down because of a lack of product definition and design. However, a complexity of 1 million or more devices per chip may be available around 1990 using 1-μm or submicron device geometries. As the channel length becomes shorter, one has to consider short-channel effects due to two-dimensional potential, high-field transport and oxide charging. Many device structures have been proposed to improve MOSFET performance. Some representative structures as well as the nonvolatile semiconductor memory, basically a MOSFET with a multilayer gate structure, will be discussed.

8.2 BASIC DEVICE CHARACTERISTICS

The basic structure of a metal–oxide–semiconductor field-effect transistor (MOSFET) is illustrated in Fig. 3. It is a four-terminal device and consists of a p-type semiconductor substrate into which two n^+ regions, the source and drain, are formed* (e.g., by ion implantation). The metal contact on the insulator is called gate; heavily doped polysilicon or a combination of silicide and polysilicon can also be used as the gate electrode. The basic device parameters are the channel length L, which is the distance between the two metallurgical n^+-p junctions; the channel width Z; the insulator thickness d; the junction depth r_j; and the substrate doping N_A. In a silicon integrated circuit, a MOSFET is surrounded by a thick oxide (called the field oxide to distinguish it from the gate oxide) to isolate it from adjacent devices.

The source contact will be used as the voltage reference throughout this

*This is an n-channel device; one may consider a p-channel device by exchanging p for n and reversing the polarity of the voltage.

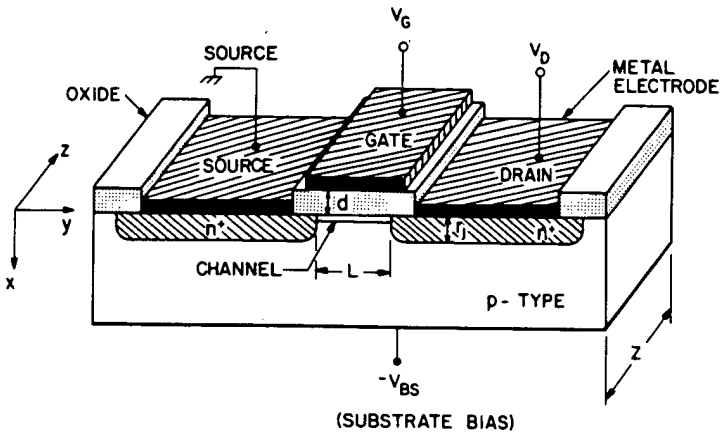

Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

chapter. When no voltage is applied to the gate, the source-to-drain electrodes correspond to two p-n junctions connected back to back. The only current that can flow from source to drain is the reverse leakage current.* When a sufficiently large positive bias is applied to the gate so that a surface inversion layer (or channel) is formed between the two n^+ regions, the source and the drain are then connected by a conducting-surface n channel through which a large current can flow. The conductance of this channel can be modulated by varying the gate voltage. The back-surface contact (or substrate contact) can have the reference voltage or be reverse-biased; the back-surface voltage will also affect the channel conductance.

8.2.1 Nonequilibrium Condition

When a voltage is applied across the source–drain contacts, the MOS structure is in a nonequilibrium condition; that is, the imref of the minority carriers (electrons, in the present case) is lowered from the equilibrium Fermi level. To show more clearly the band bending across the device, Fig. 4*a* shows[16] the MOSFET turned 90°. The two-dimensional, flat-band, zero-bias ($V_G = V_D = V_{BS} = 0$) equilibrium condition is shown in Fig. 4*b*. The equilibrium conditions under a gate bias that causes surface inversion are shown in Fig. 4*c*. The nonequilibrium condition with both drain and gate biases is shown in Fig. 4*d*, where we note the separation of the imrefs of electrons and holes; the hole imref E_{Fp} remains at the bulk Fermi level while the electron imref E_{Fn} (minority in the present case) is lowered

*This is the n-channel normally-off (enhancement-type) MOSFET. Other types will be discussed later.

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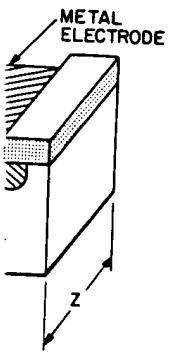

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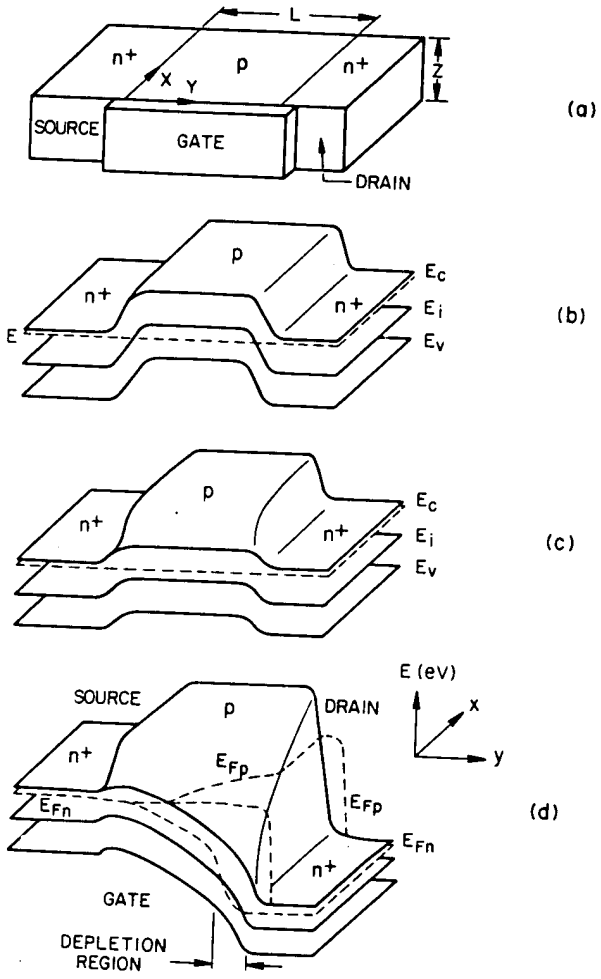


Fig. 4 Two-dimensional band diagram of an *n*-channel MOSFET. (*a*) Device configuration. (*b*) Flat-band zero-bias equilibrium condition. (*c*) Equilibrium condition under a gate bias. (*d*) Nonequilibrium condition under both gate and drain biases. (After Pao and Sah, Ref. 16.)

toward the drain contact. Figure 4*d* shows that the gate voltage required for inversion at the drain is larger than the equilibrium case in which $\psi_s(\text{inv}) \simeq 2\psi_B$. This is because the applied drain bias lowers the electron imref, and an inversion layer can be formed only when the potential at the surface crosses over the imref of the minority carrier.

Figure 5 shows a comparison[17] of the charge distribution and energy-band variation of an inverted *p* region for the equilibrium case and the nonequilibrium case at the drain. For the equilibrium case (discussed in Chapter 7), the surface depletion region reaches a maximum width W_m at

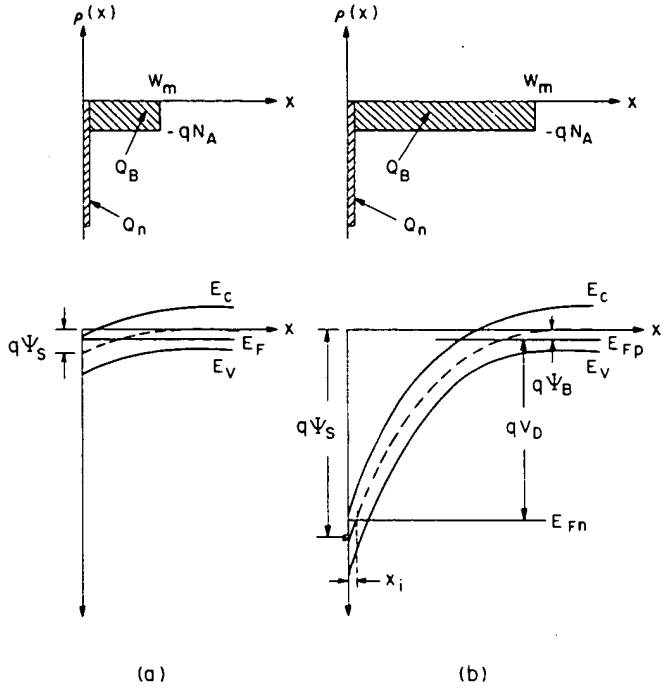


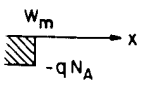
Fig. 5 Comparison of charge distribution and energy band variation of an inverted p region for (a) the equilibrium case and (b) the nonequilibrium case at the drain. (After Grove and Fitzgerald, Ref. 17.)

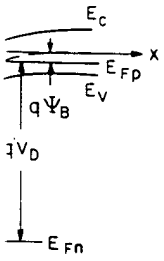
inversion. For the nonequilibrium case, the depletion-layer width is a function of the bias V_D, and the surface potential ψ_s at the onset of strong inversion is given, to a good approximation, by

$$\psi_s(\text{inv}) \simeq V_D + 2\psi_B . \tag{1}$$

The derivation for the characteristic of the surface-space charge under the nonequilibrium condition is similar to that in Chapter 7. The two assumptions are that (1) the imref for the majority carriers of the substrate does not vary with distance from the bulk to the surface, and (2) the imref for the minority carriers of the substrate is separated by the applied junction bias V_D from the imref for the majority carriers; that is, $E_{Fp} = E_{Fn} + qV_D$ for a p substrate. The first assumption introduces little error when the surface is inverted, because majority carriers are then only a negligible part of the surface space charge; the second assumption is correct under the inversion condition, because minority carriers are an important part of the surface-space-charge region when the surface is inverted.

Based on these assumptions, the one-dimensional Poisson equation for





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the surface-space-charge region at the drain is given by

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\epsilon_s}(N_D^+ - N_A^- + p - n) \tag{2}$$

where

$$N_D^+ - N_A^- = n_{po} - p_{po}, \qquad p_{po} \simeq N_A$$
$$p = p_{po}e^{-\beta\psi}$$
$$n = n_{po}e^{\beta\psi - \beta V_D}, \qquad \beta \equiv q/kT. \tag{3}$$

Following the same approach as in Chapter 7, we obtain

$$\mathscr{E} = -\frac{\partial\psi}{\partial x} = \pm\frac{\sqrt{2}kT}{qL_D}F\left(\beta\psi, V_D, \frac{n_{po}}{p_{po}}\right) \tag{4}$$

and

$$Q_s = -\epsilon_s\mathscr{E}_s = \mp\frac{\sqrt{2}\epsilon_s kT}{qL_D}F\left(\beta\psi_s, V_D, \frac{n_{po}}{p_{po}}\right) \tag{5}$$

where

$$F\left(\beta\psi, V_D, \frac{n_{po}}{p_{po}}\right) \equiv \left[e^{-\beta\psi} + \beta\psi - 1 + \frac{n_{po}}{p_{po}}e^{-\beta V_D}(e^{\beta\psi} - \beta\psi e^{\beta V_D} - 1)\right]^{1/2} \tag{6}$$

and

$$L_D \equiv \left(\frac{kT\epsilon_s}{p_{po}q^2}\right)^{1/2}. \tag{7}$$

The surface charge per unit area after strong inversion is given by

$$Q_s = Q_n + Q_B \tag{8}$$

where

$$Q_B = -qN_AW_m = -\sqrt{2qN_A\epsilon_s(V_D + 2\psi_B)} \tag{9}$$

and Q_n, the charge due to minority carriers within the inversion layer, is

$$|Q_n| \equiv q\int_0^{x_i} n(x)\,dx = q\int_{\psi_s}^{\psi_B}\frac{n(\psi)\,d\psi}{d\psi/dx} \tag{10}$$

or

$$|Q_n| = q\int_{\psi_s}^{\psi_B}\frac{n_{po}e^{(\beta\psi - \beta V_D)}\,d\psi}{(\sqrt{2}kT/qL_D)F(\beta\psi, V_D, n_{po}/p_{po})} \tag{11}$$

where x_i denotes the point at which the intrinsic Fermi level intersects the imref for electrons. For the practical doping ranges in silicon, the value of x_i is quite small, of the order of 30 to 300 Å. Equation 11 is the basic formula for long-channel MOSFET, and can be evaluated numerically.

Under strong inversion conditions, a simplified expression for Q_n can be obtained from a charge-sheet model[18] and is given by

$$|Q_n| = \sqrt{2}qN_AL_D\left\{\left[\beta\psi_s + \left(\frac{n_{po}}{p_{po}}\right)e^{(\beta\psi_s - \beta V_D)}\right]^{1/2} - (\beta\psi_s)^{1/2}\right\}. \quad (12)$$

This expression for Q_n is derived under the condition $V_{BS} = 0$. When a substrate reverse bias is applied, the depletion width increase, and the term βV_D in Eq. 12 is replaced by $\beta(V_D + V_{BS})$.

8.2.2 Linear and Saturation Regions

We shall first present a qualitative discussion of device operation. Let us consider that a voltage is applied to the gate, causing an inversion at the semiconductor surface, Fig. 6*a*. If a small drain voltage is applied, a current will flow from the source to the drain through the conducting channel. Thus the channel acts as a resistance, and the drain current I_D is proportional to the drain voltage V_D. This is the linear region. As the drain voltage increases, it eventually reaches a point at which the channel depth x_i at $y = L$ is reduced to zero; this is called the pinch-off point, Fig. 6*b*. Beyond the pinch-off point the drain current remains essentially the same, because for $V_D > V_{D\,sat}$, the voltage at Y remains the same, $V_{D\,sat}$. Thus the number of carriers arriving at point Y from the source, and hence the current flowing from source to drain, remains the same apart from a decrease in L to the value L' (Fig. 6*c*). Carrier injection from Y into the drain-depletion region is quite similar to the case of carrier injection from an emitter–base junction to the base–collector depletion region of a bipolar transistor.

We shall now derive the basic MOSFET characteristics under the following idealized conditions: (1) the gate structure corresponds to an ideal MOS diode as defined in Chapter 7; that is, there are no interface traps, fixed oxide charge, or work-function difference, and so on; (2) only drift current will be considered; (3) carrier mobility in the inversion layer is constant; (4) doping in the channel is uniform; (5) reverse leakage current is negligibly small; and (6) the transverse field ($\mathscr{E}_x$ in the x direction) in the channel is much larger than the longitudinal field ($\mathscr{E}_y$ in the y direction). The last condition corresponds to the so-called gradual channel approximation.

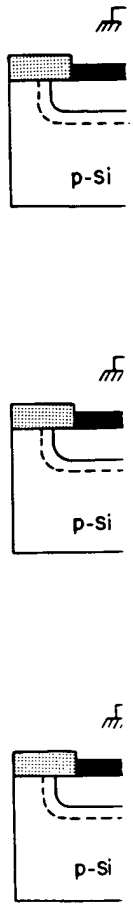
Under such idealized conditions, the total charge induced in the semiconductor per unit area Q_s at a distance y from the source is given by

$$Q_s(y) = [-V_G + \psi_s(y)]C_i \quad (13)$$

where $C_i \equiv \epsilon_i/d$ is the capacitance per unit area. The charge in the inversion layer is given by

$$\begin{aligned} Q_n(y) &= Q_s(y) - Q_B(y) \\ &= -[V_G - \psi_s(y)]C_i - Q_B(y). \end{aligned} \quad (14)$$

The surface potential $\psi_s(y)$ at inversion can be approximated by $2\psi_B +$



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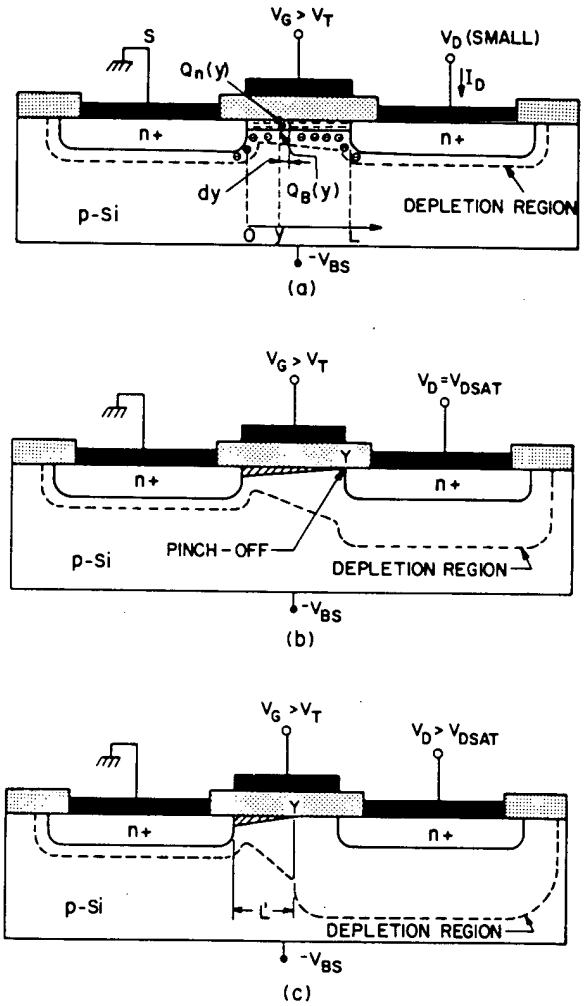

Fig. 6 (a) MOSFET operated in the linear region (low drain voltage). (*b*) MOSFET operated at onset of saturation. The point *Y* indicates the pinch-off point. (*c*) MOSFET operated beyond saturation and the effective channel length is reduced.

$V(y)$, where $V(y)$ is the reverse bias between point y and the source electrode (which is assumed to be grounded). The charge within the surface depletion region $Q_B(y)$ was given previously as

$$Q_B(y) = -qN_A W_m = -\sqrt{2\epsilon_s qN_A[V(y)+2\psi_B]}. \qquad (15)$$

Substituting Eq. 15 into Eq. 14 yields

$$Q_n(y) = -[V_G - V(y) - 2\psi_B]C_i + \sqrt{2\epsilon_s qN_A[V(y)+2\psi_B]}. \qquad (16)$$

The conductivity of the channel can be approximated by

$$\sigma(x) = qn(x)\mu_n(x). \tag{17}$$

The channel conductance is then given by

$$g = \frac{Z}{L}\int_0^{x_i} \sigma(x)\, dx. \tag{18}$$

For a constant mobility, the channel conductance becomes

$$g = \frac{qZ\mu_n}{L}\int_0^{x_i} n(x)\, dx = qZ\mu_n|Q_n|/L. \tag{19}$$

The channel resistance of an elemental section dy, Fig. 6*a*, is given by

$$dR = \frac{dy}{gL} = \frac{dy}{Z\mu_n|Q_n(y)|} \tag{20}$$

and the voltage drop across this elemental section is given by

$$dV = I_D\, dR = \frac{I_D\, dy}{Z\mu_n|Q_n(y)|} \tag{21}$$

where I_D is the drain current and is a constant independent of y. Substituting Eq. 16 into Eq. 21 and integrating from the source ($y = 0$, $V = 0$) to the drain ($y = L$, $V = V_D$) yields

$$I_D = \frac{Z}{L}\mu_n C_i\left\{\left(V_G - 2\psi_B - \frac{V_D}{2}\right)V_D - \frac{2}{3}\frac{\sqrt{2\epsilon_s qN_A}}{C_i}\left[(V_D + 2\psi_B)^{3/2} - (2\psi_B)^{3/2}\right]\right\} \tag{22}$$

for the present idealized case.

Equation 22 predicts that for a given V_G the drain current first increases linearly with drain voltage (the linear region), then gradually levels off, approaching a saturated value (the saturation region). The basic output characteristic of an idealized MOSFET is shown in Fig. 7. The dashed line indicates the locus of the drain voltage ($V_{D\,sat}$) at which the current reaches a maximum value.

We shall now consider the above-mentioned two regions. For the case of small V_D, Eq. 22 reduces to

$$I_D \simeq \frac{Z}{L}\mu_n C_i\left[(V_G - V_T)V_D - \left(\frac{1}{2} + \frac{\sqrt{\epsilon_s qN_A/\psi_B}}{4C_i}\right)V_D^2\right] \tag{23}$$

or

$$I_D \simeq \left(\frac{Z}{L}\right)\mu_n C_i(V_G - V_T)V_D \qquad \text{for} \quad V_D \ll (V_G - V_T) \tag{23a}$$

where V_T (the threshold voltage) is given by

$$V_T = 2\psi_B + \frac{\sqrt{2\epsilon_s qN_A(2\psi_B)}}{C_i}. \tag{24}$$

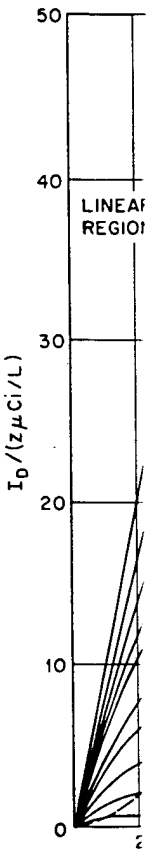

Fig. 7 Idealized drain
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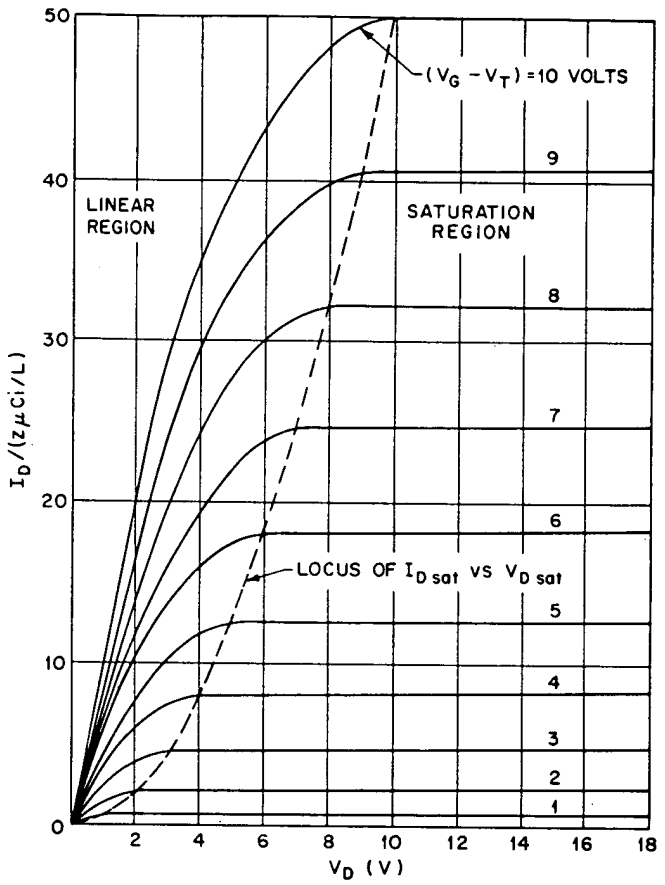

Fig. 7 Idealized drain characteristics (I_D versus V_D) of a MOSFET. The dashed line indicates the locus of the saturation drain voltage ($V_{D\,sat}$). For $V_D > V_{D\,sat}$, the drain current remains constant.

The calculated values of V_T as a function of semiconductor doping density and insulator thickness were shown in Chapter 7 for the Si–SiO_2 system. By plotting I_D versus V_G (for a given small V_D), the threshold voltage can be deduced from the linearly extrapolated value at the V_G axis. In the linear region, Eq. 23a, the channel conductance g_D and the transconductance g_m are given as

$$g_D \equiv \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G=\text{const}} = \frac{Z}{L}\mu_n C_i (V_G - V_T) \tag{25}$$

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=\text{const}} = \frac{Z}{L}\mu_n C_i V_D . \tag{26}$$

When the drain voltage is increased to a point such that the charge in the

inversion layer $Q(y)$ at $y = L$ becomes zero, the number of mobile electrons at the drain experiences a drastic fall-off. This point, called pinch-off, is analogous to the junction field-effect transistor. The drain voltage and the drain current at this point are designated as $V_{D\,sat}$ and $I_{D\,sat}$, respectively. Beyond the pinch-off point we have the saturation region. The value of $V_{D\,sat}$ is obtained from Eq. 16 under the condition $Q_n(L) = 0$:

$$V_{D\,sat} = V_G - 2\psi_B + K^2\left(1 - \sqrt{1 + 2V_G/K^2}\right) \tag{27}$$

where $K \equiv \sqrt{\epsilon_s q N_A}/C_i$. The saturation current $I_{D\,sat}$ can be obtained by substituting Eq. 27 into Eq. 22:

$$I_{D\,sat} \simeq \frac{mZ}{L}\,\mu_n C_i (V_G - V_T)^2. \tag{28}$$

where m is a function of doping concentration and approaches $\frac{1}{2}$ at low dopings.[11]

The threshold voltage V_T in the saturation region is the same as given by Eq. 24 for low substrate dopings and thin insulator layers. For higher dopings, V_T becomes V_G-dependent. The transconductance in the saturation region when Eq. 28 applies is given by

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D = \text{const.}} = \frac{2mZ}{L}\,\mu_n C_i (V_G - V_T). \tag{29}$$

In previous discussions, we made many assumptions to bring out the most important characteristics of the MOSFET. We shall now remove the first two assumptions and consider the effects due to a nonideal gate MOS and diffusion current. The main effect of the fixed oxide charges and the difference in work functions is to cause a voltage shift corresponding to the flat-band voltage V_{FB}. This in turn causes a change in the threshold voltage V_T; in the linear region V_T becomes

$$\begin{aligned} V_T &= V_{FB} + 2\psi_B + \frac{\sqrt{2\epsilon_s q N_A (2\psi_B)}}{C_i} \\ &= \left(\phi_{ms} - \frac{Q_f}{C_i}\right) + 2\psi_B + \frac{\sqrt{4\epsilon_s q N_A \psi_B}}{C_i}. \end{aligned} \tag{30}$$

When a substrate bias is applied, the threshold voltage becomes

$$V_T = V_{FB} + 2\psi_B + \sqrt{2\epsilon_s q N_A (2\psi_B + V_{BS})}/C_i \tag{31}$$

or

$$\begin{aligned} \Delta V_T &= V_T(V_{BS}) - V_T(V_{BS} = 0) \\ &= \frac{\sqrt{2\epsilon_s q N_A}}{C_i}\left(\sqrt{2\psi_B + V_{BS}} - \sqrt{2\psi_B}\right) \\ &= \frac{a}{\beta}\left(\sqrt{2\beta\psi_B + \beta V_{BS}} - \sqrt{2\beta\psi_B}\right) \end{aligned} \tag{32}$$

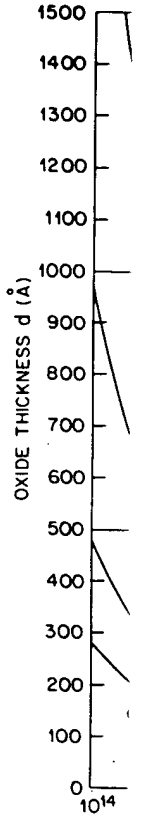

Fig. 8 Oxide thickness ve
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In Fig. 8, oxide thick
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Threshold voltage
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$$\left(\overline{+2V_G/K^2}\right) \qquad (27)$$

$I_{D\,sat}$ can be obtained by

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$$\overline{\frac{qN_A\psi_B}{C_i}}. \qquad (30)$$

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$$\overline{+ V_{BS})}/C_i \qquad (31)$$

$$\sqrt{2\psi_B}\Big)$$

$$\left.\overline{\psi_B}\right) \qquad (32)$$

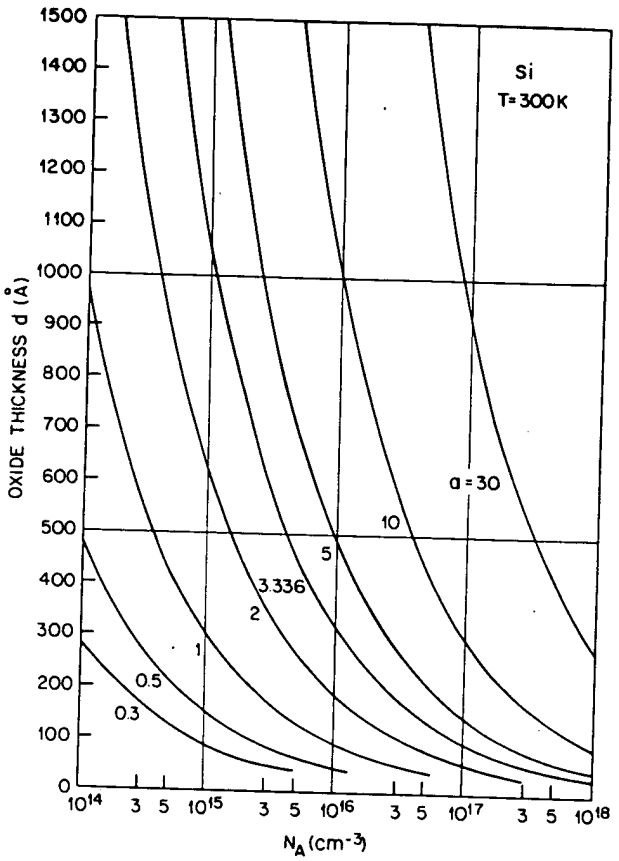

Fig. 8 Oxide thickness versus substrate doping for various a values. (After Brews, Ref. 19.)

where

$$a \equiv \sqrt{2}(\epsilon_s/L_D)/C_i = 2(\epsilon_s/\epsilon_i)(d/L_D). \qquad (33)$$

In Fig. 8, oxide thickness versus substrate doping is plotted for given a values[19] using Eq. 33. The a values increase with increasing doping and oxide thickness.

Threshold voltage shift versus V_{BS} is plotted in Fig. 9 for various a values. As the a value increases, ΔV_T also increases. For a given a value, the resulting variation in ΔV_T is indicated by vertical bars for substrate dopings ranging from 10^{15} to 10^{17} cm^{-3} (Fig. 9). The primary influence upon ΔV_T is the choice of a itself; the influence of doping or oxide thickness upon ΔV_T, independent of a, is minor.

To consider the effect of the diffusion current component, we refer to Fig. 4 for the nonequilibrium condition. The drain current density including

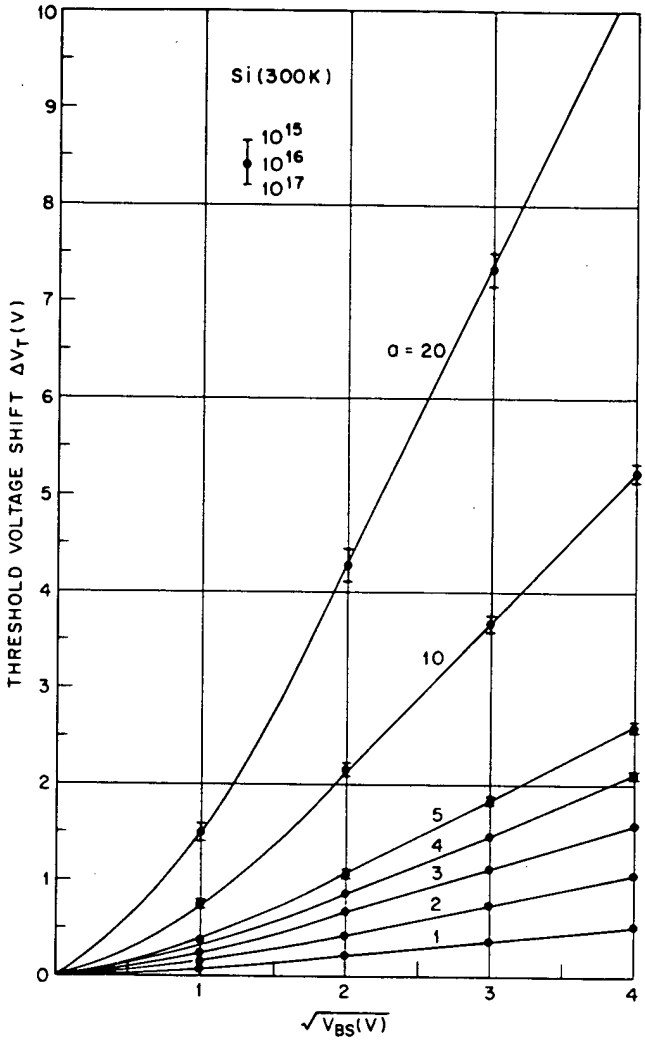

Fig. 9 Threshold voltage shift versus substrate reverse bias for various a values.

both drift and diffusion components is given by

$$J_D(x, y) = q\mu_n n\mathscr{E}_y + qD_n\nabla n$$

$$= -qD_n n(x, y)\nabla\psi_{Fn} \tag{34}$$

where ψ_{Fn} is the electron imref measured from the bulk Fermi level. The

total drain current bas

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The gate voltage V_G is

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Equation 22 however,
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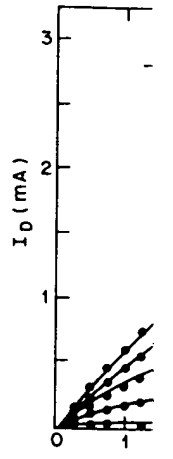
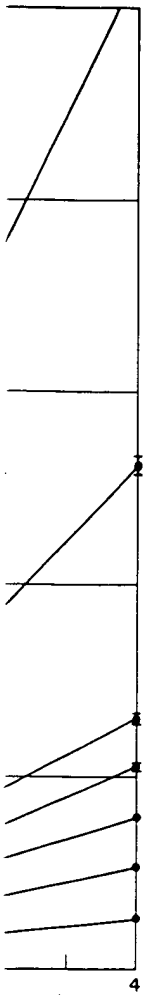


Fig. 10 Theoretical (dots
p-channel MOSFET having
Pao and Sah, Ref. 16.)



ias for various a values.

(34)

bulk Fermi level. The

total drain current based on the gradual-channel approximation is

$$I_D = \int_0^{x_i} J_D(x, y) Z \, dx$$

$$= \frac{1}{L} \int_0^L D_n q Z \left(\frac{\partial \psi_{Fn}}{\partial y} \right) \int_0^{x_i} n(x, y) \, dx \, dy$$

$$= \frac{Z}{L} \frac{\epsilon_s \mu_n}{L_D} \int_0^{V_D} \int_{\psi_B}^{\psi_s} \frac{e^{\beta\psi - \beta V}}{F(\beta\psi, V, n_{po}/p_{po})} \, d\psi \, dV. \tag{35}$$

The gate voltage V_G is related to the surface potential ψ_s by

$$V_G' = V_G - V_{FB} = -\frac{Q_s}{C_i} + \psi_s$$

$$= \frac{2\epsilon_s kT}{C_i q L_D} F\left(\beta\psi_s, V, \frac{n_{po}}{p_{po}}\right) + \psi_s . \tag{36}$$

Equation 35 reduces to Eq. 22 for gate voltages well above threshold. Equation 22 however, becomes inaccurate for gate voltages near threshold, and near pinch-off. For a particular device with known physical dimensions, bulk impurity concentration, and effective mobility, Eq. 35 can be calculated numerically to give accurate results for the entire range of drain voltage from the linear region to the saturation region. Figure 10 demonstrates the current saturation phenomena very well, showing a typical drain characteristic for a long-channel MOSFET.[16]

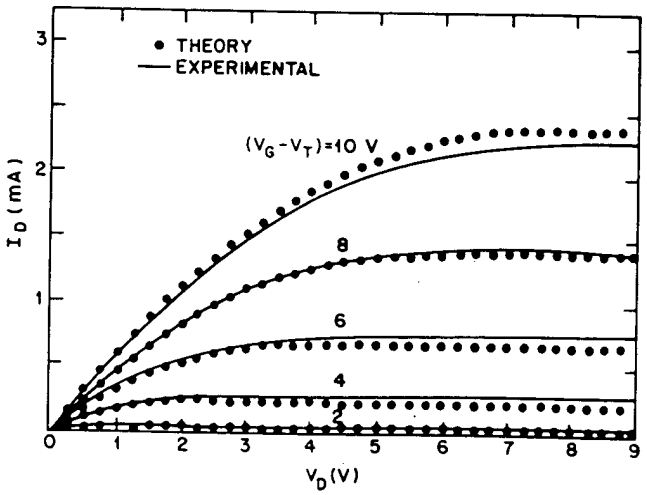
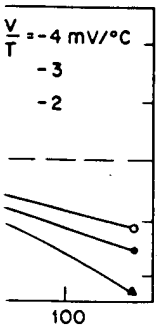
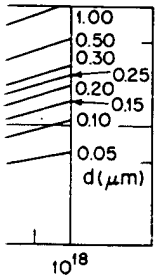


Fig. 10 Theoretical (dots) and experimental (solid lines) drain characteristics of a p-channel MOSFET having $d = 2000$ Å, $N_D = 4.6 \times 10^{14}$ cm^{-3}, and $\mu_p = 256$ cm^2/V-s. (After Pao and Sah, Ref. 16.)





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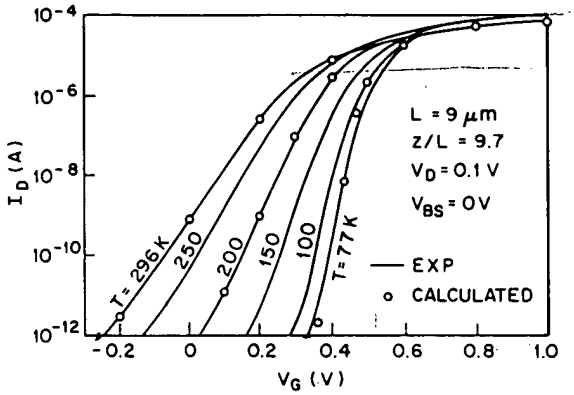


Fig. 17 Transfer characteristics for a long-channel device ($L = 9\ \mu m$) with temperature as a parameter. (After Gaensslen et al., Ref. 31.)

threshold voltage V_T increases from 0.25 V to about 0.5 V. This increase in V_T is similar to that shown in Fig. 16. The most important improvement is the reduction of the subthreshold swing S from 80 mV/decade at 296 K to 22 mV/decade at 77 K. Thus the improvement in the subthreshold swing at 77 K is about a factor of 4. This improvement comes mainly from the kT/q term in Eq. 42. Other improvements at 77 K include higher mobility, higher transconductance, higher threshold conductivity, lower power consumption, lower junction leakage current, and lower metal-line resistance. The major disadvantage is that the MOSFET must be immersed in a suitable inert coolant (e.g., liquid nitrogen) and low-temperature setup requires additional equipment.

8.2.6 Types of MOSFETs

The MOSFET is ideally a transadmittance amplifier with an infinite input resistance and a current generator at the output. In practice, however, we have other circuit parameters. An equivalent circuit is shown in Fig. 18 for the common-source connection.[32] The differential transconductance g_m was discussed previously. The input conductance G_{in} is caused by leakages through the thin gate insulator. For a thermally grown silicon dioxide layer, the leakage current between the gate and the channel is very small, of the order of 10^{-10} A/cm^2; thus the input conductance is negligible. The input capacitance C_{in} is equal to $\partial Q_M/\partial V_G$, where Q_M is the total charge on the gate.[16] In practical devices, the insulator layer and the metal gate may extend somewhat above the source and drain regions. This fringe effect will be the most important contribution to the feedback capacitance C_{fb}. The output conductance G_{out} is equal to the drain conductance. The output capacitance consists mostly of the two p-n junction capacitances connected in series through the semiconductor bulk. In the linear region, from

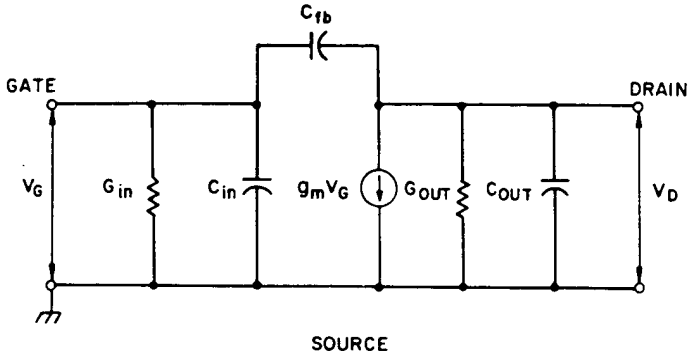


Fig. 18 Equivalent circuit of MOSFET for common-source configuration. (After Ihantola and Moll, Ref. 6.)

Eq. 26 and the fact that $C_{in} \simeq ZLC_i$, the maximum operating frequency is given by

$$f_m = \frac{\omega_m}{2\pi} = \frac{g_m}{2\pi C_{in}} \simeq \frac{\mu_n V_D}{2\pi L^2}. \tag{52}$$

In the saturation region, f_m is obtained from Eq. 49:

$$f_m \simeq \frac{v_s}{2\pi L}. \tag{53}$$

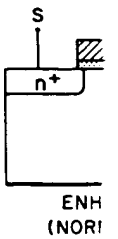
The corresponding transit time for velocity saturation is

$$\tau = \frac{L}{v_S}. \tag{54}$$

For $L = 1\ \mu$m and $v_s = 10^7$ cm/s, the transit time is only 10 ps. However, in a typical ring oscillator with 1 μm-channel MOSFETs, the measured delay time is usually an order of magnitude longer than 10 ps. Thus the delay is mainly caused by the parasitic resistance and capacitance around the device.

There are basically four different types of MOSFET, depending on the types of inversion layer. If at zero gate bias, the channel conductance is very low, we must apply positive voltage to the gate to form the n-channel. This type is the normally-off (enhancement) n-channel MOSFET. If an n-channel exists at zero bias, we must apply a negative bias to the gate to deplete carriers in the channel to reduce channel conductance. This type is called the normally-on (depletion) n-channel MOSFET. The n-channel enhancement and depletion-mode MOSFETs are shown in Fig. 19*a*. Similarly we have the p-channel normally-off (enhancement) and normally-on (depletion) MOSFET (Fig. 19*b*).

The electrical symbol, transfer characteristics, and output characteristics of the four types are shown[33] in Fig. 20. Note that for the normally-off



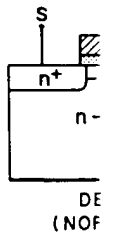
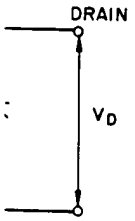


Fig. 19 B

TYPE
N-CHANNEL ENHANCEMENT (NORMALLY OFF)
N-CHANNEL DEPLETION (NORMALLY ON)
P-CHANNEL ENHANCEMENT (NORMALLY OFF)
P-CHANNEL DEPLETION (NORMALLY ON)

Fig. 20 Electric symb types of MOSFET. (Aft



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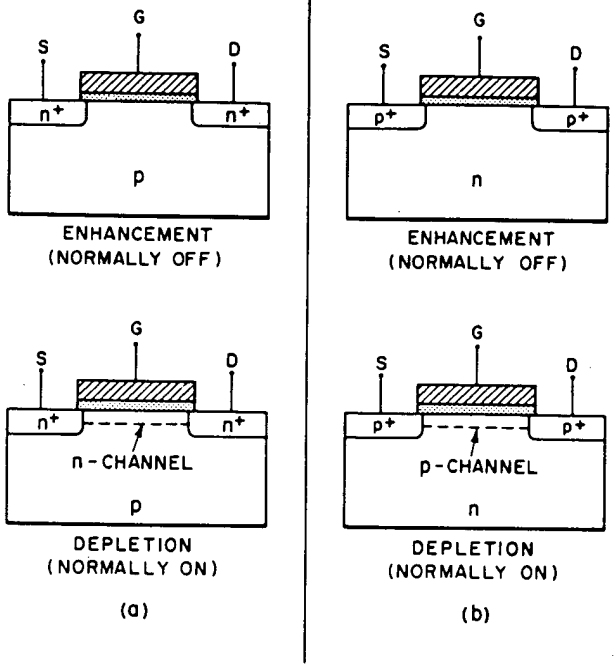


Fig. 19 Basic types of MOSFETs. (*a*) *n*-channel. (*b*) *p*-channel.

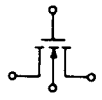
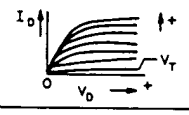
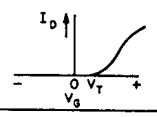
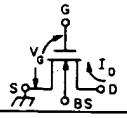
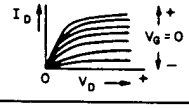
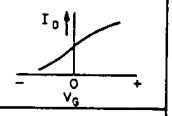
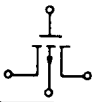
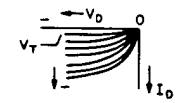
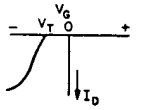
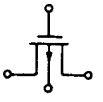
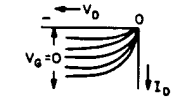
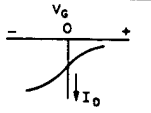
TYPE	ELECTRICAL SYMBOL	OUTPUT CHARACTERISTIC	TRANSFER CHARACTERISTIC
N-CHANNEL ENHANCEMENT (NORMALLY OFF)			
N-CHANNEL DEPLETION (NORMALLY ON)			
P-CHANNEL ENHANCEMENT (NORMALLY OFF)			
P-CHANNEL DEPLETION (NORMALLY ON)			

Fig. 20 Electric symbol, transfer characteristics, and output characteristics of the four types of MOSFET. (After Gallagher and Corak, Ref. 33.)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Philip L. Hower, et al.	Docket No:	TI-30010
Serial No:	10/036,323	Conf. No:	3224
Examiner:	Thomas L. Dickey	Art Unit:	2826
Filed:	12/31/2001		

For: N-CHANNEL LDMOS WITH BURIED P-TYPE REGION TO PREVENT PARASITIC BIPOLAR EFFECTS

APPEAL BRIEF UNDER 37 C.F.R. 1.192

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 12-12-03.

Ann Trent
Ann Trent

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed July 30, 2003, and the Advisory Action mailed October 29, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

Claims 1-13, 15, and 19-26 have been canceled. Claims 27-32 have been withdrawn. Claims 14, 16 and 18 are appealed.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

Claim 17 was amended after the final rejection. In an action dated 10/29/2003, the examiner stated that claim 17 as amended would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claims.

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

The instant invention describes a LDMOS transistor with an improved safe operating area. As shown in Figure 1 of the instant disclosure, a p-type buried body is formed beneath the source region 18 and the channel region. The channel region is represented by the region directly beneath the gate from the edge of the n+ source region 18 to the edge of the p body 20 adjacent to the isolation region 28. The n+ drain region 16 is separated from the edge of the channel region by a portion of the n-well 12.

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

1. Was claim 14 properly rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,437,399)?

2. Were claims 16 and 18 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (6,437,399) in view of Mena et al. (4,922,327)?

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

Claims 14, 16, and 18 stand or fall together.

Arguments

1. Was claim 14 properly rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,437,399)?

Appellants contend that claim 14 was not properly rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,437, 399). Claim 14 of the instant invention comprises the limitations of an n-type source diffusion, a p-type surface body diffusion which laterally surrounds at least part of said source diffusion, a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein, and a p-type buried body diffusion which underlies said channel and at least part of said surface body diffusion. In forming the rejection to claim 14, the examiner refers to region 35 as defining a p-type buried body diffusion which underlies a channel. The examiner, in the action dated 10/29/2003, defines the channel in the Huang patent (6,437,399) as being the P-type impurity region 14. This is an overbroad definition of the term "channel region" as used in claim 14 of the instant invention. The "channel region" in claim 14 is formed by, "a conductive gate structure which is capacitively coupled to part of said p–type surface body diffusion to define a channel region therein." The "channel region" of the instant invention is therefore formed when the appropriate voltages are applied to the conductive gate structure and will be confined by the existing electric fields to regions directly beneath the conductive gate structure. This definition of "channel region" coincides with the well established use of the term in semiconductor physics. Appendix I contain the pages from "Physics of Semiconductor Devices" by Sze which provide an explanation of the formation of the "channel region" and its confinement to regions beneath the conductive gate. In particular pages 433 to 445 provide the physics behind the formation of the "channel region" and Fig. 3 and Fig. 6 show the confinement of the "channel region" to the region directly beneath the conductive gate. This is also illustrated in Fig. 19 where the "channel region" is shown for various types of transistors. It should also be noted that claim 14 comprises the limitation of p-type surface body diffusion and a separate "channel region."

In describing the Huang patent, the examiner refers to region 14 in Figure 12 as a p-type surface body diffusion which laterally surrounds at least part of said source diffusion. In the action dated 10/29/2003, the examiner further explains that region 14 (which the examiner had previously equated to the p-type surface body diffusion) is now the channel region. The examiner quotes a section of the Huang patent which states "[t]he region pf P-type impurity 14, generally referred to as the base region, is herein referred to as the channel region because it is the region in which the channel forms during the operation of the device." It is a well established tenet of patent law that a patent can be its own lexicographer. In the above quoted section of the Huang patent, the patent outlines a "new" definition for the term "channel region" that is different from the well established meaning of the term as it is used in claim 14 of the instant invention. With regard to the Huang patent, examination of Figure 12 shows that the actual "channel region" as the term is used in claim 14 (i.e. the region where the channel is formed when the appropriate voltages are applied to the gate 26) extends from the edge of the N+ diffusion region 16 laterally under the gate 26 to the N type drain region. The P+ diffusion region 35 described by the examiner is positioned solely under the N+ source region 16 and does not extend under the "channel region." Therefore the term "channel region" as used in claim 14 is different from the "new" defined meaning of the term as used in the Huang patent. The "new" defined meaning of the term "channel region" applies only to the Huang patent and certainly cannot supercede the well established definition presented in Appendix I and followed in Claim 14. The examiner also refers to claim 10 in the Huang patent where it states "said channel region overlying and boarding a region of high impurity concentration." The term "channel region" in claim 10 of the Huang patent again refers to the "new" definition of the term "channel region" presented in the Huang patent.

All the limitations of claim 14 are not contained in the Huang patent and claim 14 is allowable over the cited art under 35 U.S.C. 102(e).

2. Were claims 16 and 18 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (6,437,399) in view of Mena et al. (4,922,327)?

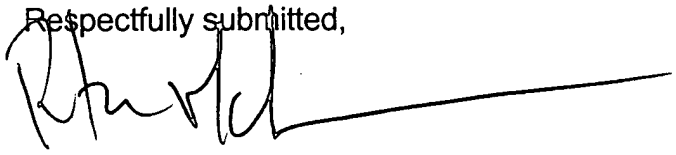
Claims 16 and 18 depend from claim 14 and therefore contain all the limitation of claim 14. The Mena et al. patent does not describe a p-type buried body diffusion which underlies said channel. As described above the Huang patent does not contain this limitation and therefore claims 16 and 18 are allowable over the Huang patent in view of the Mena et al. patent under 35 U.S.C. 103(a).

Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 14, 16, and 18 under 35 U.S.C. § 102 and 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



Peter K. McLarty
Reg. No. 44,923
Attorney for Appellants

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-4258

APPENDIX

Claims on Appeal

Claim 14: An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion, ohmically connected to a source metallization;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein;

a p-type buried body diffusion which underlies said channel and at least part of said surface body diffusion; and

an ohmic connection between said buried body diffusion and said source metallization;

whereby said buried body diffusion diverts hole current to bypass said source diffusion, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device.

Claim 16: The structure of Claim 14, further comprising a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

Claim 18: The structure of Claim 14, further comprising a drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion, and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

APPENDIX I

Physics of Semiconductor Devices

SECOND EDITION

S. M. Sze

Bell Laboratories, Incorporated
Murray Hill, New Jersey

A WILEY-INTERSCIENCE PUBLICATION

JOHN WILEY & SONS

New York • Chichester • Brisbane • Toronto • Singapore

Library of Congress Cataloging in Publication Data:

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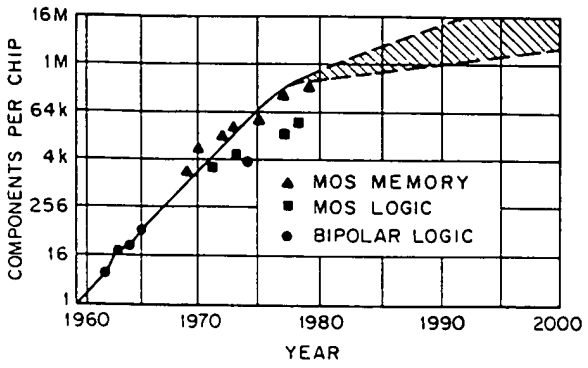


Fig. 2 Complexity of integrated circuits as a function of the year. (After Moore, Ref. 15.)

chip has grown exponentially[15] since 1959 (Fig. 2). The rate of growth is expected to slow down because of a lack of product definition and design. However, a complexity of 1 million or more devices per chip may be available around 1990 using 1-μm or submicron device geometries. As the channel length becomes shorter, one has to consider short-channel effects due to two-dimensional potential, high-field transport and oxide charging. Many device structures have been proposed to improve MOSFET performance. Some representative structures as well as the nonvolatile semiconductor memory, basically a MOSFET with a multilayer gate structure, will be discussed.

8.2 BASIC DEVICE CHARACTERISTICS

The basic structure of a metal–oxide–semiconductor field-effect transistor (MOSFET) is illustrated in Fig. 3. It is a four-terminal device and consists of a p-type semiconductor substrate into which two n^+ regions, the source and drain, are formed* (e.g., by ion implantation). The metal contact on the insulator is called gate; heavily doped polysilicon or a combination of silicide and polysilicon can also be used as the gate electrode. The basic device parameters are the channel length L, which is the distance between the two metallurgical n^+-p junctions; the channel width Z; the insulator thickness d; the junction depth r_j; and the substrate doping N_A. In a silicon integrated circuit, a MOSFET is surrounded by a thick oxide (called the field oxide to distinguish it from the gate oxide) to isolate it from adjacent devices.

The source contact will be used as the voltage reference throughout this

*This is an n-channel device; one may consider a p-channel device by exchanging p for n and reversing the polarity of the voltage.

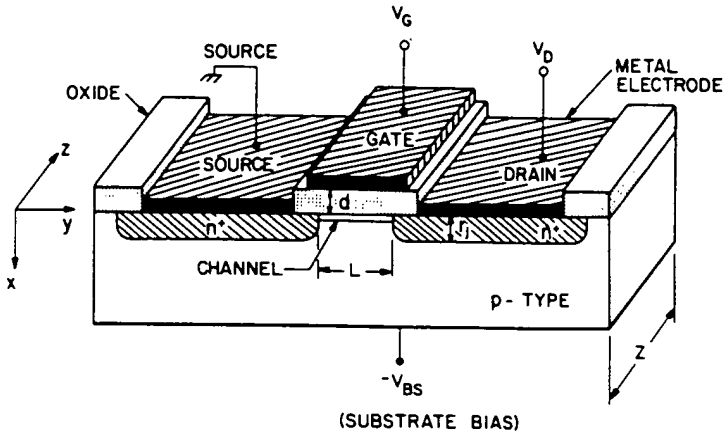


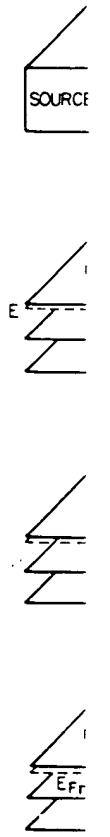
Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

chapter. When no voltage is applied to the gate, the source-to-drain electrodes correspond to two p-n junctions connected back to back. The only current that can flow from source to drain is the reverse leakage current.* When a sufficiently large positive bias is applied to the gate so that a surface inversion layer (or channel) is formed between the two n^+ regions, the source and the drain are then connected by a conducting-surface n channel through which a large current can flow. The conductance of this channel can be modulated by varying the gate voltage. The back-surface contact (or substrate contact) can have the reference voltage or be reverse-biased; the back-surface voltage will also affect the channel conductance.

8.2.1 Nonequilibrium Condition

When a voltage is applied across the source–drain contacts, the MOS structure is in a nonequilibrium condition; that is, the imref of the minority carriers (electrons, in the present case) is lowered from the equilibrium Fermi level. To show more clearly the band bending across the device, Fig. 4*a* shows[16] the MOSFET turned 90°. The two-dimensional, flat-band, zero-bias ($V_G = V_D = V_{BS} = 0$) equilibrium condition is shown in Fig. 4*b*. The equilibrium conditions under a gate bias that causes surface inversion are shown in Fig. 4*c*. The nonequilibrium condition with both drain and gate biases is shown in Fig. 4*d*, where we note the separation of the imrefs of electrons and holes; the hole imref E_{Fp} remains at the bulk Fermi level while the electron imref E_{Fn} (minority in the present case) is lowered

*This is the n-channel normally-off (enhancement-type) MOSFET. Other types will be discussed later.



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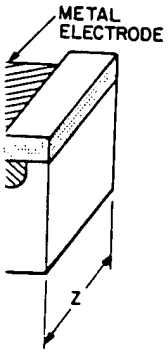

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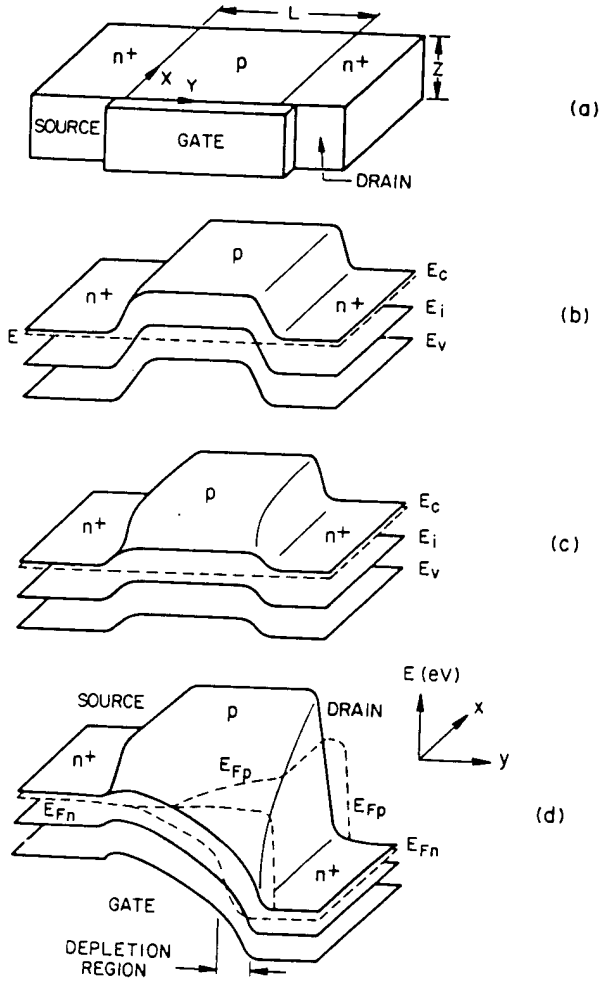

Fig. 4 Two-dimensional band diagram of an *n*-channel MOSFET. (a) Device configuration. (*b*) Flat-band zero-bias equilibrium condition. (c) Equilibrium condition under a gate bias. (*d*) Nonequilibrium condition under both gate and drain biases. (After Pao and Sah, Ref. 16.)

toward the drain contact. Figure 4*d* shows that the gate voltage required for inversion at the drain is larger than the equilibrium case in which $\psi_s(\text{inv}) \simeq 2\psi_B$. This is because the applied drain bias lowers the electron imref, and an inversion layer can be formed only when the potential at the surface crosses over the imref of the minority carrier.

Figure 5 shows a comparison[17] of the charge distribution and energy-band variation of an inverted *p* region for the equilibrium case and the nonequilibrium case at the drain. For the equilibrium case (discussed in Chapter 7), the surface depletion region reaches a maximum width W_m at

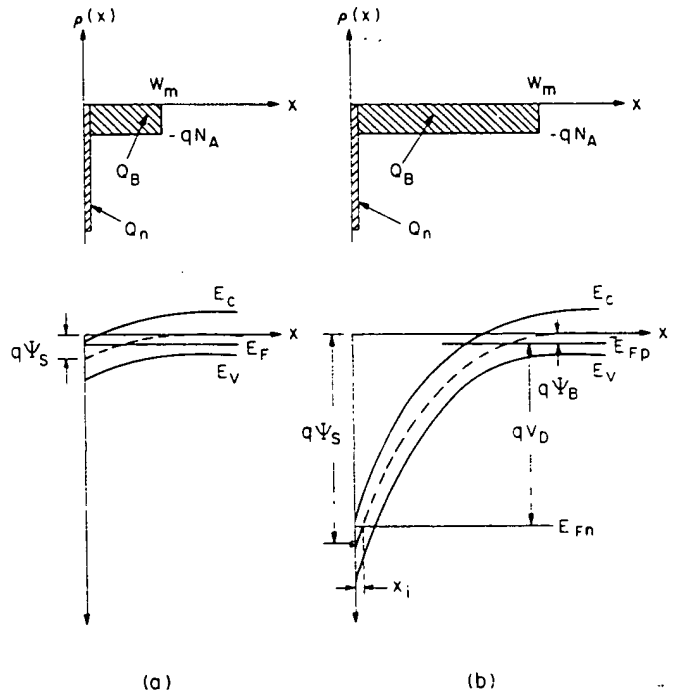

Fig. 5 Comparison of charge distribution and energy band variation of an inverted p region for (a) the equilibrium case and (b) the nonequilibrium case at the drain. (After Grove and Fitzgerald, Ref. 17.)

inversion. For the nonequilibrium case, the depletion-layer width is a function of the bias V_D, and the surface potential ψ_s at the onset of strong inversion is given, to a good approximation, by

$$\psi_s(\text{inv}) \simeq V_D + 2\psi_B . \tag{1}$$

The derivation for the characteristic of the surface-space charge under the nonequilibrium condition is similar to that in Chapter 7. The two assumptions are that (1) the imref for the majority carriers of the substrate does not vary with distance from the bulk to the surface, and (2) the imref for the minority carriers of the substrate is separated by the applied junction bias V_D from the imref for the majority carriers; that is, $E_{Fp} = E_{Fn} + qV_D$ for a p substrate. The first assumption introduces little error when the surface is inverted, because majority carriers are then only a negligible part of the surface space charge; the second assumption is correct under the inversion condition, because minority carriers are an important part of the surface-space-charge region when the surface is inverted.

Based on these assumptions, the one-dimensional Poisson equation for

the surface-space-char

where

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and

Q_s =

where

$F\left(\beta\psi, V_D, \frac{n_{po}}{p_{po}}\right)$

and

The surface charge p

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and Q_n, the charge d

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or

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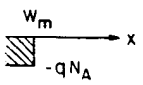

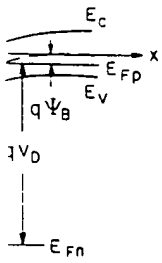

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the surface-space-charge region at the drain is given by

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\epsilon_s}(N_D^+ - N_A^- + p - n) \tag{2}$$

where

$$N_D^+ - N_A^- = n_{po} - p_{po}, \qquad p_{po} \simeq N_A$$
$$p = p_{po}e^{-\beta\psi}$$
$$n = n_{po}e^{\beta\psi - \beta V_D}, \qquad \beta \equiv q/kT. \tag{3}$$

Following the same approach as in Chapter 7, we obtain

$$\mathscr{E} = -\frac{\partial\psi}{\partial x} = \pm\frac{\sqrt{2}kT}{qL_D}F\left(\beta\psi, V_D, \frac{n_{po}}{p_{po}}\right) \tag{4}$$

and

$$Q_s = -\epsilon_s\mathscr{E}_s = \mp\frac{\sqrt{2}\epsilon_s kT}{qL_D}F\left(\beta\psi_s, V_D, \frac{n_{po}}{p_{po}}\right) \tag{5}$$

where

$$F\left(\beta\psi, V_D, \frac{n_{po}}{p_{po}}\right) \equiv \left[e^{-\beta\psi} + \beta\psi - 1 + \frac{n_{po}}{p_{po}}e^{-\beta V_D}(e^{\beta\psi} - \beta\psi e^{\beta V_D} - 1)\right]^{1/2} \tag{6}$$

and

$$L_D \equiv \left(\frac{kT\epsilon_s}{p_{po}q^2}\right)^{1/2}. \tag{7}$$

The surface charge per unit area after strong inversion is given by

$$Q_s = Q_n + Q_B \tag{8}$$

where

$$Q_B = -qN_A W_m = -\sqrt{2qN_A\epsilon_s(V_D + 2\psi_B)} \tag{9}$$

and Q_n, the charge due to minority carriers within the inversion layer, is

$$|Q_n| \equiv q\int_0^{x_i} n(x)\,dx = q\int_{\psi_s}^{\psi_B}\frac{n(\psi)\,d\psi}{d\psi/dx} \tag{10}$$

or

$$|Q_n| = q\int_{\psi_s}^{\psi_B}\frac{n_{po}e^{(\beta\psi - \beta V_D)}\,d\psi}{(\sqrt{2}kT/qL_D)F(\beta\psi, V_D, n_{po}/p_{po})} \tag{11}$$

where x_i denotes the point at which the intrinsic Fermi level intersects the imref for electrons. For the practical doping ranges in silicon, the value of x_i is quite small, of the order of 30 to 300 Å. Equation 11 is the basic formula for long-channel MOSFET, and can be evaluated numerically.

Under strong inversion conditions, a simplified expression for Q_n can be obtained from a charge-sheet model[18] and is given by

$$|Q_n| = \sqrt{2}qN_A L_D \left\{ \left[\beta\psi_s + \left(\frac{n_{po}}{p_{po}}\right) e^{(\beta\psi_s - \beta V_D)} \right]^{1/2} - (\beta\psi_s)^{1/2} \right\}. \quad (12)$$

This expression for Q_n is derived under the condition $V_{BS} = 0$. When a substrate reverse bias is applied, the depletion width increase, and the term βV_D in Eq. 12 is replaced by $\beta(V_D + V_{BS})$.

8.2.2 Linear and Saturation Regions

We shall first present a qualitative discussion of device operation. Let us consider that a voltage is applied to the gate, causing an inversion at the semiconductor surface, Fig. 6*a*. If a small drain voltage is applied, a current will flow from the source to the drain through the conducting channel. Thus the channel acts as a resistance, and the drain current I_D is proportional to the drain voltage V_D. This is the linear region. As the drain voltage increases, it eventually reaches a point at which the channel depth x_i at $y = L$ is reduced to zero; this is called the pinch-off point, Fig. 6*b*. Beyond the pinch-off point the drain current remains essentially the same, because for $V_D > V_{D\,sat}$, the voltage at Y remains the same, $V_{D\,sat}$. Thus the number of carriers arriving at point Y from the source, and hence the current flowing from source to drain, remains the same apart from a decrease in L to the value L' (Fig. 6*c*). Carrier injection from Y into the drain-depletion region is quite similar to the case of carrier injection from an emitter–base junction to the base–collector depletion region of a bipolar transistor.

We shall now derive the basic MOSFET characteristics under the following idealized conditions: (1) the gate structure corresponds to an ideal MOS diode as defined in Chapter 7; that is, there are no interface traps, fixed oxide charge, or work-function difference, and so on; (2) only drift current will be considered; (3) carrier mobility in the inversion layer is constant; (4) doping in the channel is uniform; (5) reverse leakage current is negligibly small; and (6) the transverse field ($\mathscr{E}_x$ in the x direction) in the channel is much larger than the longitudinal field ($\mathscr{E}_y$ in the y direction). The last condition corresponds to the so-called gradual channel approximation.

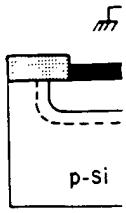
Under such idealized conditions, the total charge induced in the semiconductor per unit area Q_s at a distance y from the source is given by

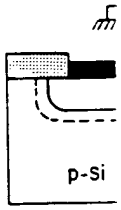
$$Q_s(y) = [-V_G + \psi_s(y)]C_i \quad (13)$$

where $C_i \equiv \epsilon_i/d$ is the capacitance per unit area. The charge in the inversion layer is given by

$$\begin{aligned} Q_n(y) &= Q_s(y) - Q_B(y) \\ &= -[V_G - \psi_s(y)]C_i - Q_B(y). \end{aligned} \quad (14)$$

The surface potential $\psi_s(y)$ at inversion can be approximated by $2\psi_B +$





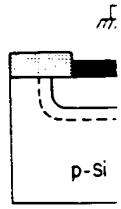


Fig. 6 (a) MOSFET ope
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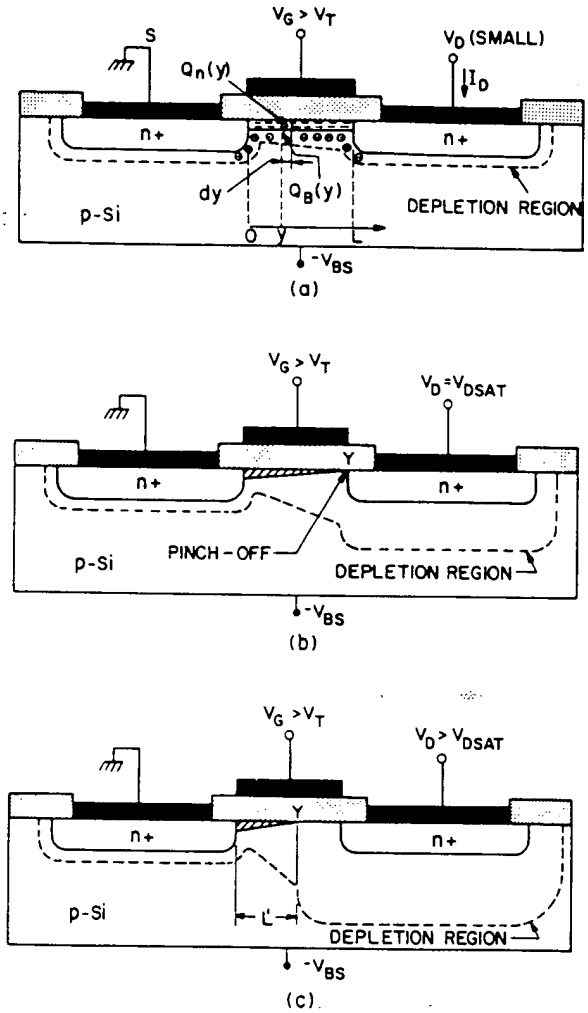

Fig. 6 (a) MOSFET operated in the linear region (low drain voltage). (*b*) MOSFET operated at onset of saturation. The point *Y* indicates the pinch-off point. (c) MOSFET operated beyond saturation and the effective channel length is reduced.

$V(y)$, where $V(y)$ is the reverse bias between point y and the source electrode (which is assumed to be grounded). The charge within the surface depletion region $Q_B(y)$ was given previously as

$$Q_B(y) = -qN_A W_m = -\sqrt{2\epsilon_s qN_A[V(y) + 2\psi_B]}. \qquad (15)$$

Substituting Eq. 15 into Eq. 14 yields

$$Q_n(y) = -[V_G - V(y) - 2\psi_B]C_i + \sqrt{2\epsilon_s qN_A[V(y) + 2\psi_B]}. \qquad (16)$$

The conductivity of the channel can be approximated by

$$\sigma(x) = qn(x)\mu_n(x). \tag{17}$$

The channel conductance is then given by

$$g = \frac{Z}{L}\int_0^{x_i} \sigma(x)\,dx. \tag{18}$$

For a constant mobility, the channel conductance becomes

$$g = \frac{qZ\mu_n}{L}\int_0^{x_i} n(x)\,dx = qZ\mu_n|Q_n|/L. \tag{19}$$

The channel resistance of an elemental section dy, Fig. 6*a*, is given by

$$dR = \frac{dy}{gL} = \frac{dy}{Z\mu_n|Q_n(y)|} \tag{20}$$

and the voltage drop across this elemental section is given by

$$dV = I_D\,dR = \frac{I_D\,dy}{Z\mu_n|Q_n(y)|} \tag{21}$$

where I_D is the drain current and is a constant independent of y. Substituting Eq. 16 into Eq. 21 and integrating from the source ($y = 0$, $V = 0$) to the drain ($y = L$, $V = V_D$) yields

$$I_D = \frac{Z}{L}\mu_n C_i\left\{\left(V_G - 2\psi_B - \frac{V_D}{2}\right)V_D - \frac{2}{3}\frac{\sqrt{2\epsilon_s qN_A}}{C_i}\left[(V_D + 2\psi_B)^{3/2} - (2\psi_B)^{3/2}\right]\right\} \tag{22}$$

for the present idealized case.

Equation 22 predicts that for a given V_G the drain current first increases linearly with drain voltage (the linear region), then gradually levels off, approaching a saturated value (the saturation region). The basic output characteristic of an idealized MOSFET is shown in Fig. 7. The dashed line indicates the locus of the drain voltage ($V_{D\,sat}$) at which the current reaches a maximum value.

We shall now consider the above-mentioned two regions. For the case of small V_D, Eq. 22 reduces to

$$I_D \simeq \frac{Z}{L}\mu_n C_i\left[(V_G - V_T)V_D - \left(\frac{1}{2} + \frac{\sqrt{\epsilon_s qN_A/\psi_B}}{4C_i}\right)V_D^2\right] \tag{23}$$

or

$$I_D \simeq \left(\frac{Z}{L}\right)\mu_n C_i(V_G - V_T)V_D \qquad \text{for} \quad V_D \ll (V_G - V_T) \tag{23a}$$

where V_T (the threshold voltage) is given by

$$V_T = 2\psi_B + \frac{\sqrt{2\epsilon_s qN_A(2\psi_B)}}{C_i}. \tag{24}$$

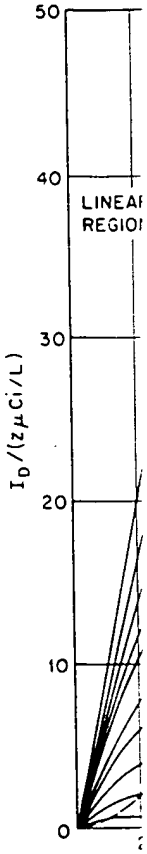

Fig. 7 Idealized drain
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$$\left.\left(\frac{\sqrt{\quad}}{\sqrt{\psi_B}}\right) V_D^2\right] \qquad (23)$$

$$\ll (V_G - V_T) \qquad (23a)$$

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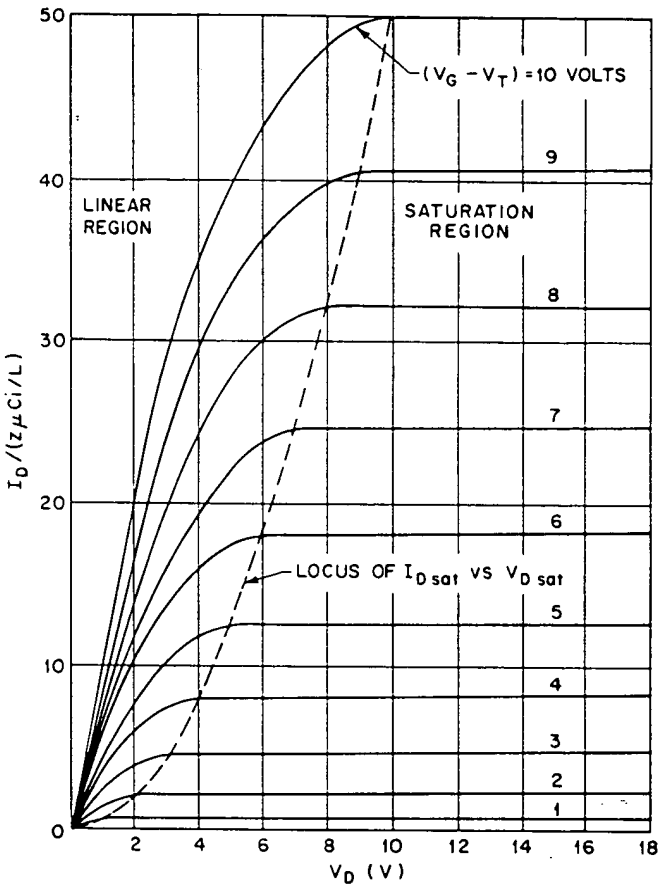

Fig. 7 Idealized drain characteristics (I_D versus V_D) of a MOSFET. The dashed line indicates the locus of the saturation drain voltage ($V_{D\,sat}$). For $V_D > V_{D\,sat}$, the drain current remains constant.

The calculated values of V_T as a function of semiconductor doping density and insulator thickness were shown in Chapter 7 for the Si–SiO_2 system. By plotting I_D versus V_G (for a given small V_D), the threshold voltage can be deduced from the linearly extrapolated value at the V_G axis. In the linear region, Eq. 23a, the channel conductance g_D and the transconductance g_m are given as

$$g_D \equiv \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G=\text{const}} = \frac{Z}{L}\mu_n C_i (V_G - V_T) \qquad (25)$$

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=\text{const}} = \frac{Z}{L}\mu_n C_i V_D . \qquad (26)$$

When the drain voltage is increased to a point such that the charge in the

inversion layer $Q(y)$ at $y = L$ becomes zero, the number of mobile electrons at the drain experiences a drastic fall-off. This point, called pinch-off, is analogous to the junction field-effect transistor. The drain voltage and the drain current at this point are designated as $V_{D\,sat}$ and $I_{D\,sat}$, respectively. Beyond the pinch-off point we have the saturation region. The value of $V_{D\,sat}$ is obtained from Eq. 16 under the condition $Q_n(L) = 0$:

$$V_{D\,sat} = V_G - 2\psi_B + K^2\left(1 - \sqrt{1 + 2V_G/K^2}\right) \tag{27}$$

where $K \equiv \sqrt{\epsilon_s qN_A}/C_i$. The saturation current $I_{D\,sat}$ can be obtained by substituting Eq. 27 into Eq. 22:

$$I_{D\,sat} \approx \frac{mZ}{L}\mu_n C_i (V_G - V_T)^2. \tag{28}$$

where m is a function of doping concentration and approaches $\frac{1}{2}$ at low dopings.[11]

The threshold voltage V_T in the saturation region is the same as given by Eq. 24 for low substrate dopings and thin insulator layers. For higher dopings, V_T becomes V_G-dependent. The transconductance in the saturation region when Eq. 28 applies is given by

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D = \text{const.}} = \frac{2mZ}{L}\mu_n C_i (V_G - V_T). \tag{29}$$

In previous discussions, we made many assumptions to bring out the most important characteristics of the MOSFET. We shall now remove the first two assumptions and consider the effects due to a nonideal gate MOS and diffusion current. The main effect of the fixed oxide charges and the difference in work functions is to cause a voltage shift corresponding to the flat-band voltage V_{FB}. This in turn causes a change in the threshold voltage V_T; in the linear region V_T becomes

$$\begin{aligned} V_T &= V_{FB} + 2\psi_B + \frac{\sqrt{2\epsilon_s qN_A(2\psi_B)}}{C_i} \\ &= \left(\phi_{ms} - \frac{Q_f}{C_i}\right) + 2\psi_B + \frac{\sqrt{4\epsilon_s qN_A\psi_B}}{C_i}. \end{aligned} \tag{30}$$

When a substrate bias is applied, the threshold voltage becomes

$$V_T = V_{FB} + 2\psi_B + \sqrt{2\epsilon_s qN_A(2\psi_B + V_{BS})}/C_i \tag{31}$$

or

$$\begin{aligned} \Delta V_T &= V_T(V_{BS}) - V_T(V_{BS} = 0) \\ &= \frac{\sqrt{2\epsilon_s qN_A}}{C_i}\left(\sqrt{2\psi_B + V_{BS}} - \sqrt{2\psi_B}\right) \\ &= \frac{a}{\beta}\left(\sqrt{2\beta\psi_B + \beta V_{BS}} - \sqrt{2\beta\psi_B}\right) \end{aligned} \tag{32}$$

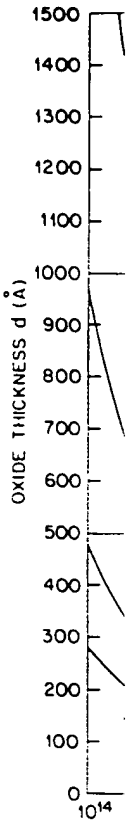

Fig. 8 Oxide thickness ve
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In Fig. 8, oxide thick
values[19] using Eq. 33.
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Threshold voltage
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$$\left(+ 2V_G/K^2\right) \qquad (27)$$

$I_{D\,sat}$ can be obtained by

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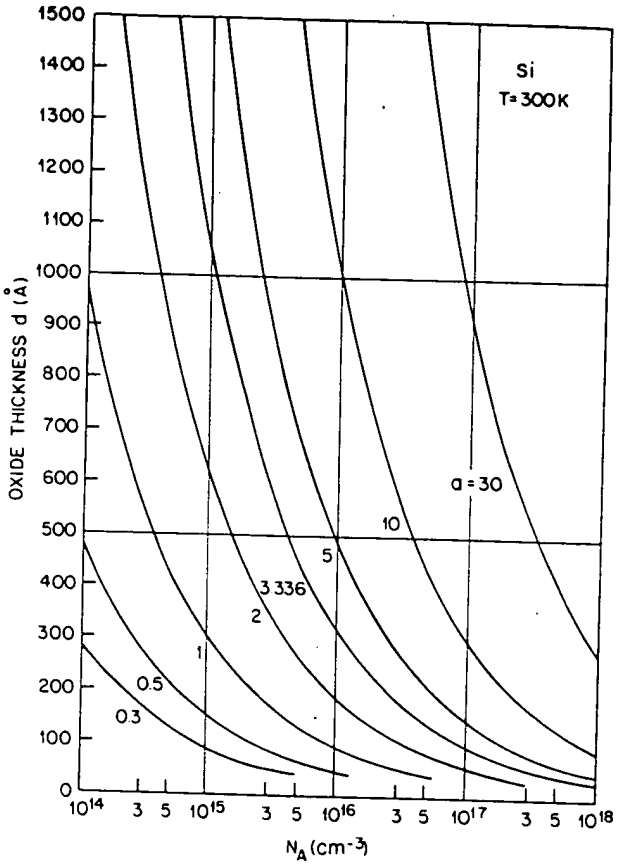

Fig. 8 Oxide thickness versus substrate doping for various a values. (After Brews, Ref. 19.)

where

$$a \equiv \sqrt{2}(\epsilon_s/L_D)/C_i = 2(\epsilon_s/\epsilon_i)(d/L_D). \qquad (33)$$

In Fig. 8, oxide thickness versus substrate doping is plotted for given a values[19] using Eq. 33. The a values increase with increasing doping and oxide thickness.

Threshold voltage shift versus V_{BS} is plotted in Fig. 9 for various a values. As the a value increases, ΔV_T also increases. For a given a value, the resulting variation in ΔV_T is indicated by vertical bars for substrate dopings ranging from 10^{15} to $10^{17}\,cm^{-3}$ (Fig. 9). The primary influence upon ΔV_T is the choice of a itself; the influence of doping or oxide thickness upon ΔV_T, independent of a, is minor.

To consider the effect of the diffusion current component, we refer to Fig. 4 for the nonequilibrium condition. The drain current density including

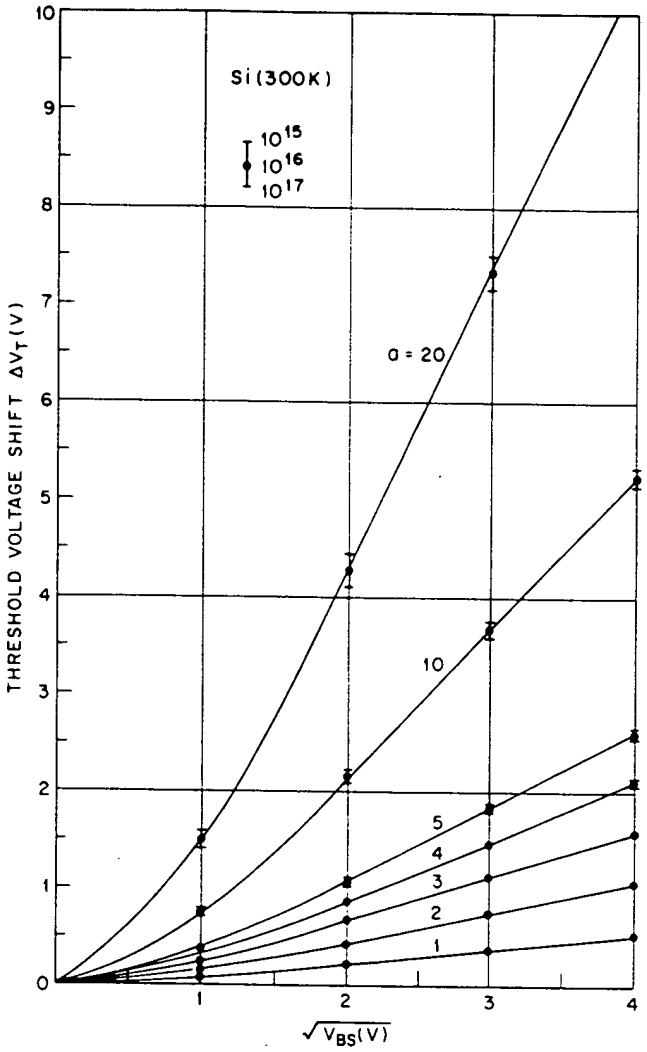

Fig. 9 Threshold voltage shift versus substrate reverse bias for various a values.

both drift and diffusion components is given by

$$J_D(x, y) = q\mu_n n\mathscr{E}_y + qD_n\nabla n$$

$$= -qD_n n(x, y)\nabla\psi_{Fn} \tag{34}$$

where ψ_{Fn} is the electron imref measured from the bulk Fermi level. The

total drain current bas

$$I_D =$$

$$=$$

$$=$$

The gate voltage V_G is

Equation 35 reduces
Equation 22 however,
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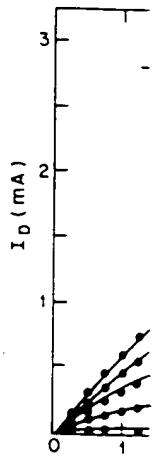
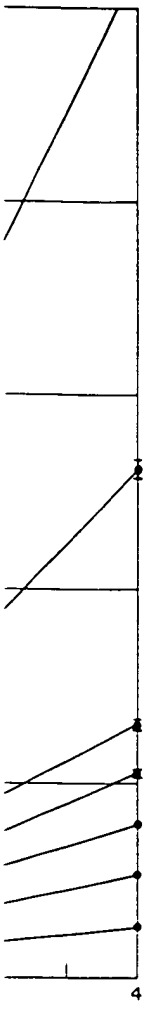


Fig. 10 Theoretical (dots
p-channel MOSFET having
Pao and Sah, Ref. 16.)



ias for various a values.

(34)

bulk Fermi level. The

total drain current based on the gradual-channel approximation is

$$I_D = \int_0^{x_i} J_D(x, y) Z \, dx$$

$$= \frac{1}{L} \int_0^L D_n q Z \left(\frac{\partial \psi_{Fn}}{\partial y} \right) \int_0^{x_i} n(x, y) \, dx \, dy$$

$$= \frac{Z}{L} \frac{\epsilon_s \mu_n}{L_D} \int_0^{V_D} \int_{\psi_B}^{\psi_s} \frac{e^{\beta\psi - \beta V}}{F(\beta\psi, V, n_{po}/p_{po})} \, d\psi \, dV. \tag{35}$$

The gate voltage V_G is related to the surface potential ψ_s by

$$V_G' = V_G - V_{FB} = -\frac{Q_s}{C_i} + \psi_s$$

$$= \frac{2\epsilon_s kT}{C_i q L_D} F\left(\beta\psi_s, V, \frac{n_{po}}{p_{po}}\right) + \psi_s . \tag{36}$$

Equation 35 reduces to Eq. 22 for gate voltages well above threshold. Equation 22 however, becomes inaccurate for gate voltages near threshold, and near pinch-off. For a particular device with known physical dimensions, bulk impurity concentration, and effective mobility, Eq. 35 can be calculated numerically to give accurate results for the entire range of drain voltage from the linear region to the saturation region. Figure 10 demonstrates the current saturation phenomena very well, showing a typical drain characteristic for a long-channel MOSFET.[16]

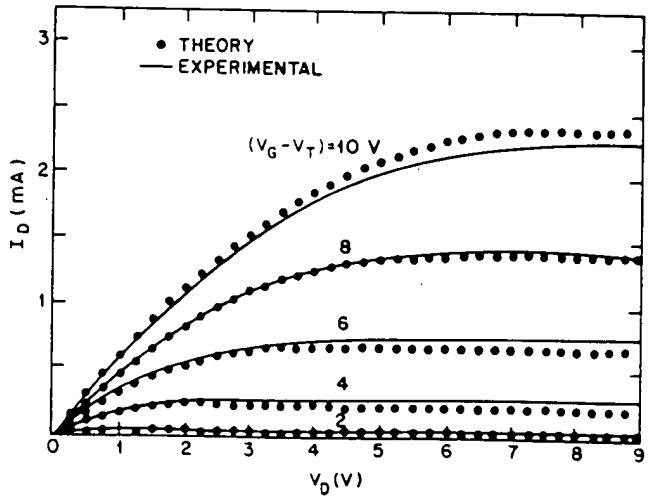
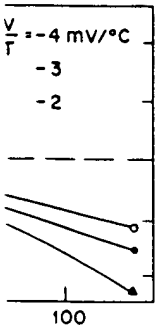
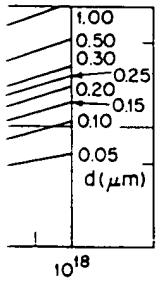


Fig. 10 Theoretical (dots) and experimental (solid lines) drain characteristics of a p-channel MOSFET having $d = 2000$ Å, $N_D = 4.6 \times 10^{14}$ cm^{-3}, and $\mu_p = 256$ cm^2/V-s. (After Pao and Sah, Ref. 16.)





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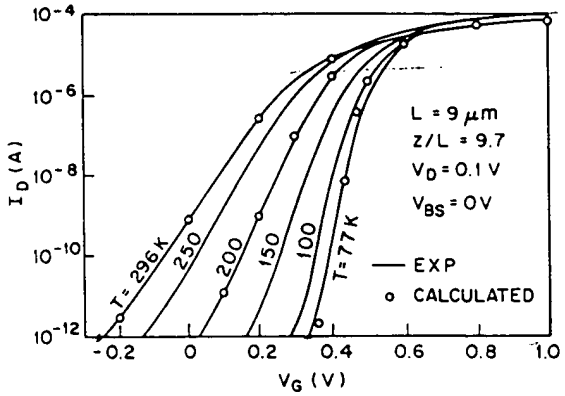


Fig. 17 Transfer characteristics for a long-channel device ($L = 9\ \mu m$) with temperature as a parameter. (After Gaensslen et al., Ref. 31.)

threshold voltage V_T increases from 0.25 V to about 0.5 V. This increase in V_T is similar to that shown in Fig. 16. The most important improvement is the reduction of the subthreshold swing S from 80 mV/decade at 296 K to 22 mV/decade at 77 K. Thus the improvement in the subthreshold swing at 77 K is about a factor of 4. This improvement comes mainly from the kT/q term in Eq. 42. Other improvements at 77 K include higher mobility, higher transconductance, higher threshold conductivity, lower power consumption, lower junction leakage current, and lower metal-line resistance. The major disadvantage is that the MOSFET must be immersed in a suitable inert coolant (e.g., liquid nitrogen) and low-temperature setup requires additional equipment.

8.2.6 Types of MOSFETs

The MOSFET is ideally a transadmittance amplifier with an infinite input resistance and a current generator at the output. In practice, however, we have other circuit parameters. An equivalent circuit is shown in Fig. 18 for the common-source connection.[32] The differential transconductance g_m was discussed previously. The input conductance G_{in} is caused by leakages through the thin gate insulator. For a thermally grown silicon dioxide layer, the leakage current between the gate and the channel is very small, of the order of 10^{-10} A/cm^2; thus the input conductance is negligible. The input capacitance C_{in} is equal to $\partial Q_M/\partial V_G$, where Q_M is the total charge on the gate.[16] In practical devices, the insulator layer and the metal gate may extend somewhat above the source and drain regions. This fringe effect will be the most important contribution to the feedback capacitance C_{fb}. The output conductance G_{out} is equal to the drain conductance. The output capacitance consists mostly of the two p-n junction capacitances connected in series through the semiconductor bulk. In the linear region, from

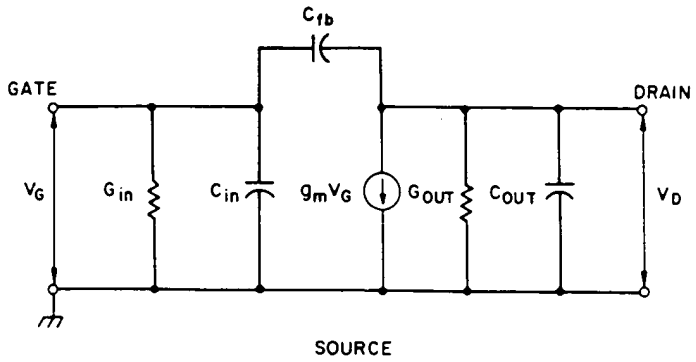


Fig. 18 Equivalent circuit of MOSFET for common-source configuration. (After Ihantola and Moll, Ref. 6.)

Eq. 26 and the fact that $C_{in} \simeq ZLC_i$, the maximum operating frequency is given by

$$f_m = \frac{\omega_m}{2\pi} = \frac{g_m}{2\pi C_{in}} \simeq \frac{\mu_n V_D}{2\pi L^2}. \tag{52}$$

In the saturation region, f_m is obtained from Eq. 49:

$$f_m \simeq \frac{v_s}{2\pi L}. \tag{53}$$

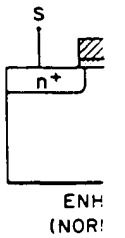
The corresponding transit time for velocity saturation is

$$\tau = \frac{L}{v_S}. \tag{54}$$

For $L = 1\ \mu$m and $v_s = 10^7$ cm/s, the transit time is only 10 ps. However, in a typical ring oscillator with 1 μm-channel MOSFETs, the measured delay time is usually an order of magnitude longer than 10 ps. Thus the delay is mainly caused by the parasitic resistance and capacitance around the device.

There are basically four different types of MOSFET, depending on the types of inversion layer. If at zero gate bias, the channel conductance is very low, we must apply positive voltage to the gate to form the n-channel. This type is the normally-off (enhancement) n-channel MOSFET. If an n-channel exists at zero bias, we must apply a negative bias to the gate to deplete carriers in the channel to reduce channel conductance. This type is called the normally-on (depletion) n-channel MOSFET. The n-channel enhancement and depletion-mode MOSFETs are shown in Fig. 19*a*. Similarly we have the p-channel normally-off (enhancement) and normally-on (depletion) MOSFET (Fig. 19*b*).

The electrical symbol, transfer characteristics, and output characteristics of the four types are shown[33] in Fig. 20. Note that for the normally-off



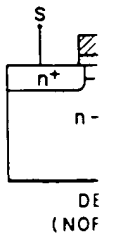


Fig. 19 B

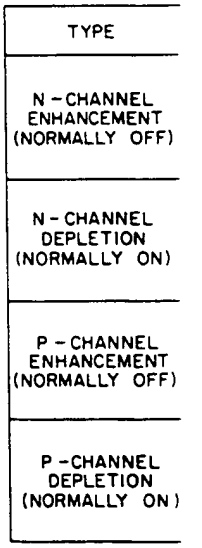
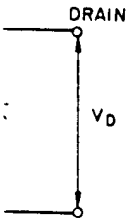


Fig. 20 Electric symb types of MOSFET. (Aft



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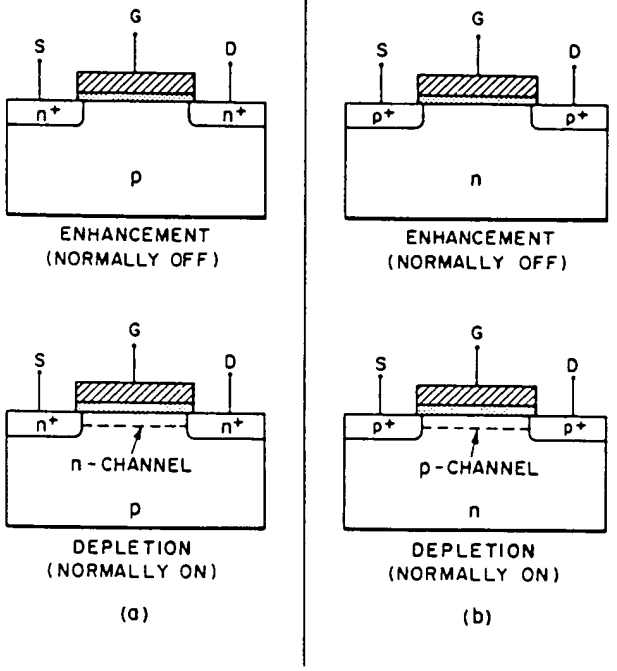


Fig. 19 Basic types of MOSFETs. (*a*) *n*-channel. (*b*) *p*-channel.

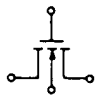
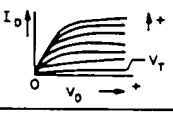
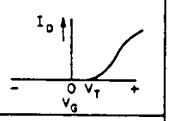
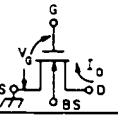
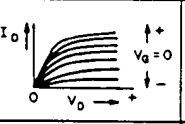
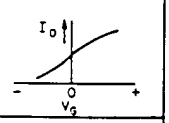
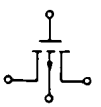
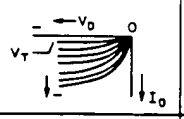
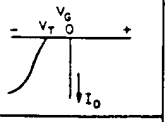
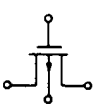
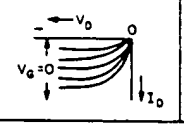
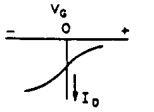
TYPE	ELECTRICAL SYMBOL	OUTPUT CHARACTERISTIC	TRANSFER CHARACTERISTIC
N-CHANNEL ENHANCEMENT (NORMALLY OFF)			
N-CHANNEL DEPLETION (NORMALLY ON)			
P-CHANNEL ENHANCEMENT (NORMALLY OFF)			
P-CHANNEL DEPLETION (NORMALLY ON)			

Fig. 20 Electric symbol, transfer characteristics, and output characteristics of the four types of MOSFET. (After Gallagher and Corak, Ref. 33.)